

EAST - [10786798.wsp:1]

File View Edit Tools Window Help

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L4: (65482) split near gate near flash near memory or EEPROM\$1 or (electrically near erasable nea...
 L3: (65482) split near gate near flash near memory or EEPROM\$1 or (electrically near erasable nea...
 L5: (946) 3 and floating near gate near insulat\$3
 L6: (251) 3 and floating near gate near insulat\$3 and control near gate and spacer

S1: (65482) split near gate near flash near memory or EEPROM\$1 or (electrically near erasable nea...
 S2: (64549) split near gate near flash near memory or EEPROM\$1 or split-gate near memory or split...
 S4: (1) S3 and intergate near insulator
 S3: (601) S2 and (floating near gate) and control near gate and spacer\$1 and gate near insulat\$3...
 S5: (74) S1 and intergate near insulat\$3

Patch L4 Browse Queue
 Data US-PG-PLB USPAT, EPO... ☐ Patch
 Default operator: OR ☒ Highlight all items initially
 3 and floating near gate near insulat\$3 and control near gate and spacer

BRS form IS&R form Image Test HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
20	<input type="checkbox"/>	<input type="checkbox"/>	US 20040171243 A1	20040902	20	Method of forming a conductive pattern of a semiconductor device and method of	438/593	438/585
21	<input type="checkbox"/>	<input type="checkbox"/>	US 20040171217 A1	20040902	21	Method of manufacturing a non-volatile semiconductor memory	438/257	
22	<input type="checkbox"/>	<input type="checkbox"/>	US 20040152268 A1	20040805	9	Method of manufacturing a floating gate and method of manufacturing a non-volatile semiconductor memory device comprising the same	438/266	438/257; 438/258
23	<input type="checkbox"/>	<input type="checkbox"/>	US 20040151021 A1	20040805	14	Novel method of fabricating split gate flash memory cell without select gate-to-drain bridging	365/149	
24	<input type="checkbox"/>	<input type="checkbox"/>	US 20040135193 A1	20040715	19	Nonvolatile memory capable of storing multibits binary information and the method of forming the same	257/315	
25	<input type="checkbox"/>	<input type="checkbox"/>	US 20040132250 A1	20040708	75	Cell structure of EPROM device and method for fabricating the same	438/264	257/E21.682; 257/E27.103; 257/E29.129
26	<input type="checkbox"/>	<input type="checkbox"/>	US 20040132248 A1	20040708	11	Preventing dielectric thickening over a gate area of a transistor	438/257	257/E21.209; 257/E29.129
27	<input type="checkbox"/>	<input type="checkbox"/>	US 20040130947 A1	20040708	31	Flash memory cell and method for fabricating the same	365/185.05	365/51
28	<input type="checkbox"/>	<input type="checkbox"/>	US 20040119112 A1	20040624	12	Flash memory with trench select gate and fabrication process	257/316	257/E21.209; 257/E21.689; 257/E27.081
29	<input type="checkbox"/>	<input type="checkbox"/>	US 20040106259 A1	20040603	12	Multi-level memory cell with lateral floating spacers	438/267	257/E21.682; 257/E27.103
30	<input type="checkbox"/>	<input type="checkbox"/>	US 20040105319 A1	20040603	25	High coupling split-gate transistor	365/199	257/E21.422; 257/E21.682; 257/E29.316
						METHOD OF MANUFACTURING A SCALABLE FLASH EEPROM MEMORY CELL WITH FLOATING GATE SPACER WRAPPED BY CONTROL GATE		

☒ No ☐ Data ☒ HTML

Ready